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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,034	09/03/2003	SU TAO	10231-US-PA	2033

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
HA, NATHAN W	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,034	TAO ET AL.	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The disclosure is objected to because of the following informalities:

The phrase "Figs. 2 –8" should be changed to "Figures 2 and 4-8", in section [0018], line 1. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 5, 7-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakayama (US 2003/0164549).

In regard to claims 1 and 9, in figs.20-21, Nakayama discloses a chip package structure process, comprising:

providing a matrix substrate 10, [0068], line 1;

disposing a plurality of chips 20 (semiconductor chip) on the matrix substrate and the chips are electrically connected to the matrix substrate, [0070] and fig. 20;

disposing a stiffener 122 (heat sink) on the matrix substrate [0121], wherein the stiffener includes an outer surface and an opposite inner surface and the inner surface of the stiffener faces the matrix substrate;

providing a molding compound 51, or sealant [0086] to cover the chips, the matrix substrate, the outer surface and the inner surface of the stiffener, fig. 21; and

dicing the molding compound, the matrix substrate and the stiffener to form a plurality of chip package structures. See [0118-0119]. Fig. 21 also shows the wafer after being separated in individual chips.

In regard to claims 2 and 10, Nakayama further discloses wherein the stiffener has a plurality of openings and locations of the openings correspond to locations of the chips disposed on the matrix substrate. See fig. 20.

In regard to claims 3 and 11, wherein the inner surface of the stiffener faces the chips. See fig. 20.

In regard to claim 5, Nakayama further discloses wherein a plurality of solder balls 52 are formed on the matrix substrate after dicing the molding compound, the matrix substrate and the stiffener. See figs. 20-21.

In regard to claims 7 and 12, Nakayama further discloses that wherein the chips are attached to the matrix substrate through an adhesive in the step of disposing the plurality of chips ([0073], line 6) and a plurality of wires 24 are formed by wire-bonding to electrically connect the chips and the matrix substrate. See [0074].

In regard to claims 8 and 13, wherein a material of the stiffener is copper. See [0075].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama as applied to claims 1-3, 5, and 7-13 above, and further in view of Wang et al., US 5,977,626, hereinafter, Wang.

In regard to claims 4, 20 and 22, Nakayama discloses all of the claimed limitations as mentioned above except the stiffener being attached to the substrate through an adhesive layer.

Wang, in fig. 2, discloses an analogous semiconductor package including a substrate 20, a chip 22 disposed on the substrate electrically through wiring 26, and a stiffener, heat sink, that is attached to the substrate using adhesive 34. The heat sink further includes a surrounding sidewall, and a flange portion that extends outwardly

from the sidewall (as cited in claim 22) at the bottom where the heat sink and the substrate are in contact. This structure provides support and secure the heat sink to the substrate to prevent the heat sink from moving during process of encapsulating the package.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to prolong the heat sink and secure it to the substrate by adhesive in order to provide support and secure the heat sink to the substrate to preventing the heat sink from moving during process of encapsulating the package. It is further noted that adhesive is used to prevent the moisture at the gap between the substrate and the heat sink.

In regard to claim 21, please see above discussions regarding to claim 2.

In regard to claim 23, please the above discussions regarding to claim 8, wherein the heat sink is made out of copper.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama as applied to claims 1-3, 5, and 7-13 above.

In regard to claim 6, the above discussions of one embodiment in Nakayama discloses all of the claimed limitations as cited in the instant claim 1. However, this embodiment does not disclose that wherein a plurality of solder balls are formed on the substrate before the dicing step. Nakayama, however, further discloses another embodiment, fig. 4, which discloses the solder balls are formed on the matrix substrate before dicing the molding compound. This process allows all the external connections,

for example, 52 and 16, be formed in one step, therefore, excellent productivity is achieved. See [0084].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply the reverse steps as taught by an embodiment, fig.4, to perform the dicing at the end of the process in order to form all of the external connections in one single step since it is common to dice the wafer at the end. Furthermore, the process of applying the solder balls to the back of the whole wafer before the dicing can be carried out quicker, instead of each chip individually (after the dicing).

9. Claims 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama, above cited reference.

In regard to claim 14, Nakayama discloses all of the claimed limitations as mentioned above except the thickness of the substrate.

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the thickness of the substrate because applicant has not disclosed that this thickness provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with either thickness because they perform the same function of positioning the module to the substrate.

Therefore, it would have been obvious to one of ordinary skill in the art to modify Nakayama to obtain the invention as specify in the above claim.

Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

In regard to claim 15, see the above discussions regarding to claim 1, wherein the stiffener is covered in the molding compound.

In regard to claim 16, see the above discussions regarding to claim 3, wherein the inner surface of the stiffener faces the chip.

In regard to claim 17, see the above discussions regarding to claim 2, wherein the stiffener has openings.

In regard to claim 18, Nakayama further discloses a plurality of wires 24 and the chip disposed on the substrate is electrically connected to the substrate through the wires. See fig. 20 and section [0074].

In regard to claim 19, see the above discussions regarding to claim 13, wherein the stiffener is made of copper.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nathan W. Ha

Nathan Ha
July 29, 2004